Amendments to the Claims

Claim 1. (Cancelled).

Claim 2. (Canceled).

Claim 3. (Currently Amended) The delay time adjusting circuit as claimed in claim 7, wherein said phase comparison circuit supplies a signal indicating said comparison result to said delay adjusting circuit according to said signal generated by said second divider and obtained via said dummy circuit.

Claims 4 to 6. (Cancelled).

Claim 7. (Currently Amended) A delay time adjusting circuit receiving an input signal for outputting an output signal by adjusting a delay time of said input signal, comprising:

a first divider configured to divide a frequency of said input signal by a first division rate;

a variable delay circuit, including a delay chain in which delay units are coupled in series, configured to delay said input signal by selecting a number of said delay units to output said output signal;

a second divider configured to divide a frequency of said output signal by a second division rate higher than said first division rate;

a dummy circuit configured to delay a signal from said second divider by a fixed delay time;

a phase comparison circuit configured to compare phases of ~~signals~~ a signal from said first ~~and second dividers~~ divider and a signal from said dummy circuit; and

a delay adjusting circuit configured to select the number of said delay units in response to a comparison result in said phase comparison circuit.

Claim 8. (Currently Amended) A delay time adjusting circuit receiving an input signal for outputting an output signal by adjusting a delay time of said input signal, comprising:

a variable delay circuit, including a delay chain in which delay units are coupled in series, configured to delay said input signal by selecting a number of said delay units to output said output signal;

a divider configured to divide a frequency of said output signal by a division rate, wherein a frequency of a signal from said ~~driver~~ divider is less than a frequency of said input signal;

a dummy circuit configured to delay a signal from said divider by a fixed delay time;

a phase comparison circuit configured to compare phases of said input signal and said signal from said ~~divider~~ dummy circuit; and

a delay adjusting circuit configured to select the number of said delay units in response to a comparison result in said phase comparison circuit.

Claim 9. (Currently Amended) A delay time adjusting method for receiving an input signal and outputting an output signal by adjusting a delay time of said input signal, comprising the steps of:

(a) dividing a frequency of said input signal by a first division rate;

(b) using a delay chain in which delay units are coupled in series and delaying said input signal by selecting a number of said delay units to output said output signal;

(c) dividing a frequency of said output signal by a second division rate higher than said first division rate;

(d) delaying a signal obtained by said step (c) by a fixed delay time;

~~(d)~~ (e) comparing phases of signals obtained by said steps (a) and ~~(c)~~ (d); and

~~(e)~~ (f) selecting the number of said delay units in response to a comparison result in said step ~~(d)~~ (e).

Claim 10. (Currently Amended) A delay time adjusting method for receiving an input signal and outputting an output signal by adjusting a delay time of said input signal, comprising the steps of:

(a) using a delay chain in which delay units are coupled in series and delaying said input signal by selecting a number of said delay units to output said output signal;

(b) dividing a frequency of said output signal by a division rate, wherein a frequency of a signal ~~from said divider~~ obtained by said step (b) is less than a frequency of said input signal;

(c) delaying the signal obtained by said step (b) by a fixed delay time;

~~(c)~~ (d) comparing phases of said input signal and ~~said~~ the signal obtained by said step ~~(b)~~ (c); and

~~(d)~~ (e) selecting the number of said delay units in response to a comparison result in said step ~~(c)~~ (d).

Claim 11. (Currently Amended) The delay time adjusting method as claimed in claim 9, wherein said step ~~(d)~~ (e) supplies a signal indicating said comparison result to said step ~~(e)~~ (f) according to said signal generated by said step (c) and obtained via said step (d).